REMARKS

Amendments

Amendments to the Claims

Applicant has canceled claims 1, 10, 15 and 22 without prejudice. No new matter has been added as a result of these amendments.

Rejections

Rejections under 35 U.S.C. § 102(b)

Claims 2 and 9

Claims 2 and 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Rao, WO 97/06523. Applicant respectfully submits that Rao does not teach each and every element of the invention as claimed in claims 2 and 9.

Rao discloses a unified system and frame buffer memory system using a single memory controller where the frame buffer and system (i.e. main) memory are collocated in a single integrated circuit or single bank of circuits (Rao, Figure 1, unified memory #105). Because Rao's frame buffer consists of screen update and refresh buffers, the screen update and refresh buffers are in a single integrated circuit or single bank of circuits. Rao contrasts the unified system with the prior art that used two memory controllers and where the frame buffer is physically separate from the system memory. Furthermore, Rao discloses that the unified memory system overcomes inefficiencies presented with separate memory devices.

With regards to claim 2, Applicant claims a sole memory controller that maps addresses for frame-preparation memory onto the main memory and refresh memory onto a physical memory device separate from the main memory. The Examiner equates Applicant's frame-preparation and refresh memory to Rao's screen update and refresh buffer, respectively. However, Rao discloses (i) a unified memory system with one memory controller that collocates screen update and refresh buffers onto single bank of circuits or a single integrated circuit (Rao, p. 11, lines 26-29) and (ii) prior art that has two memory controllers that maps the frame buffer on memory that is physically separate

from the system memory. Neither disclosure of Rao teaches or suggests a sole memory controller that maps frame-preparation memory onto the main memory and refresh memory onto a physical memory device separate from the main memory as claimed. Furthermore, it would not be obvious to combine Rao with Rao's prior art because Rao discloses that physically separate memory devices is inefficient. Thus, Rao does not teach or suggest the claimed element and cannot be properly interpreted as disclosing the claimed element in claim 2 and claim 9 that depends on claim 2. Therefore, Applicant respectfully submits that the invention as claimed in claims 2 and 9 is not anticipated by Rao under 35 U.S.C. § 102(e) and respectfully requests the withdrawal of the rejection of the claims.

Rejections under 35 U.S.C. § 103(a)

Claims 3-8, 11-14, 16-21 and 23-26

Claims 3-8, 11-14, 16-21 and 23-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Rao in view of Akeley, US Patent No. 6,075,543. Applicant respectfully submits that the combination does not teach each and every element of the invention as claimed in claims 3-8, 11-14, 16-21 and 23-26.

Akeley discloses managing multiple frame buffers by maintaining a queue of buffers. However, Akeley does not disclose how the buffers are mapped onto physical or graphics memories.

Applicant respectfully submits that the combination of Rao and Akeley does not support a *prima facie* case of obviousness because the combination does not teach or suggest each and every limitation of Applicant's invention as claimed in claims 3-8, 11-14, 16-21 and 23-26. Claims 3-8 depend from independent claim 2. Furthermore, like claim 2, claims 11, 16 and 23 claim a sole memory controller that maps addresses for frame-preparation memory onto the main memory and refresh memory onto a physical memory device separate from the main memory. Thus, Akeley must disclose at the least the missing element from claims 2, 11, 16, and 23 in order to have a proper *prima facie* case for claims 3-8, 11-14, 16-21 and 23-26.

However, there is no disclosure in Akeley that teaches or suggests a sole memory controller that maps addresses for frame-preparation memory onto the main memory and refresh memory onto a physical memory device separate from the main memory. In

contrast, Akeley discloses managing multiple buffers. As neither Rao nor Akeley teach or suggest this element as claimed in claims 2, 11, 16 and 23, the combination cannot be interpreted as disclosing claims 2, 11, 16 and 23 and claims 3-8, 12-14, 17-21 and 24-26 that depend on them, respectively. Therefore, the combination cannot render obvious Applicant's invention as claimed in claims 3-8, 11-14, 16-21 and 23-26, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

SUMMARY

Claims 2-9, 11-14, 16-21 and 23-26 are currently pending. In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Eric Replogle at (408) 720-8300 x258.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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